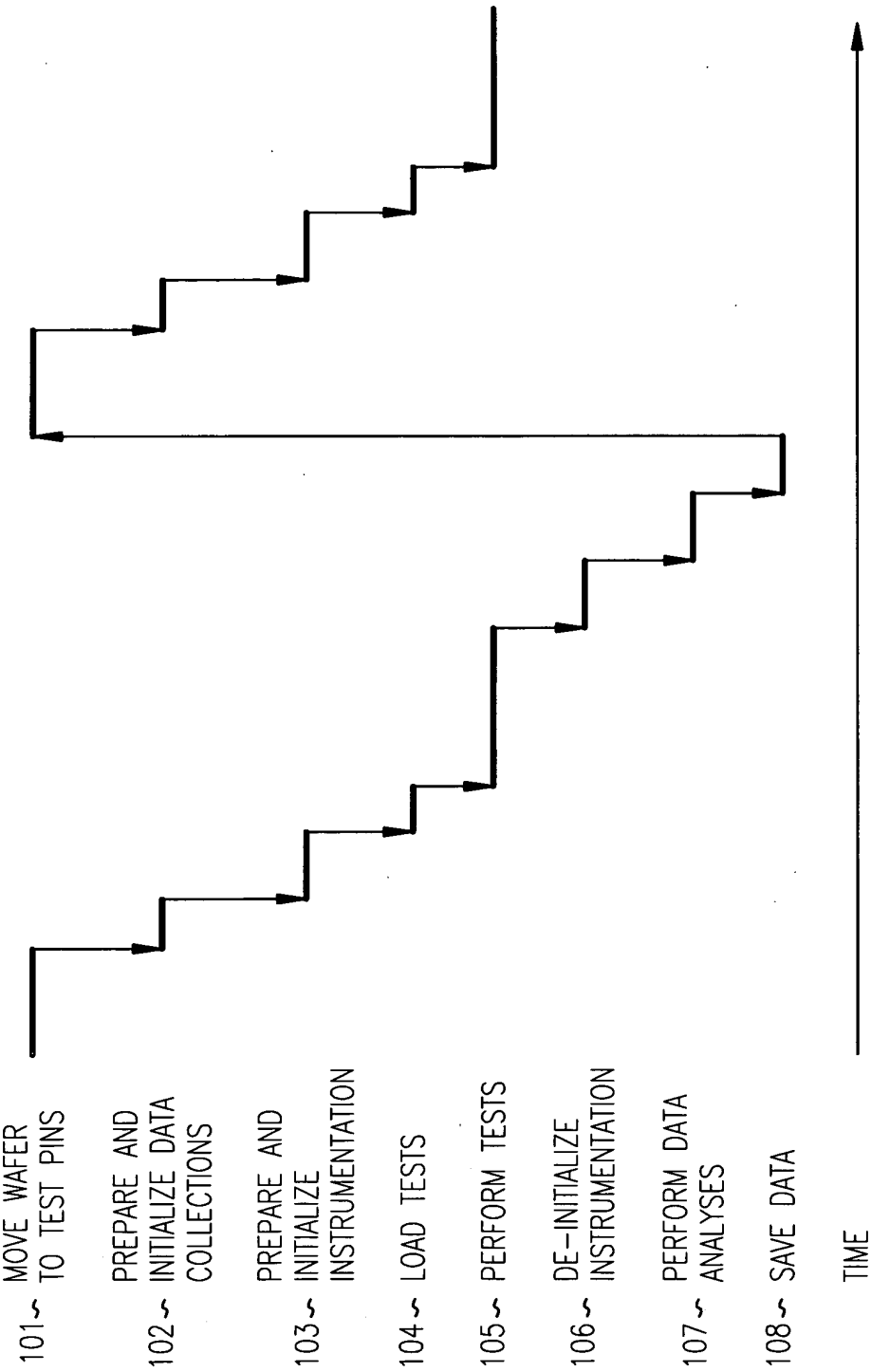


FIG. 1
(PRIOR ART)

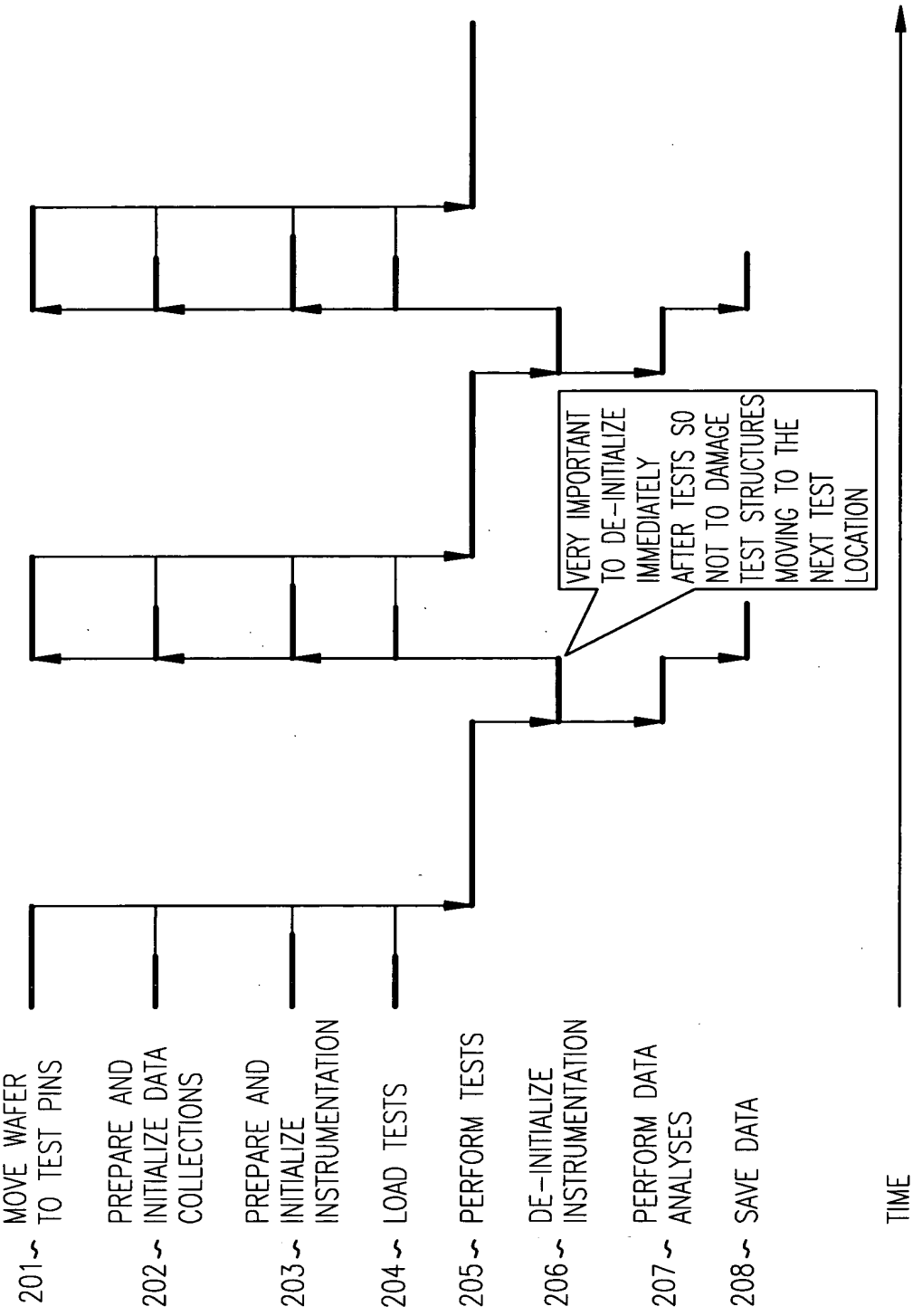

201 MOVE WAFER TO TEST PINS
202 PREPARE AND INITIALIZE DATA COLLECTIONS
203 PREPARE AND INITIALIZE INSTRUMENTATION
204 LOAD TESTS
205 PERFORM TESTS
206 DE-INITIALIZE INSTRUMENTATION
207 PERFORM DATA ANALYSES
208 SAVE DATA
TIME
VERY IMPORTANT TO DE-INITIALIZE IMMEDIATELY AFTER TESTS SO NOT TO DAMAGE TEST STRUCTURES MOVING TO THE NEXT TEST LOCATION

FIG. 2

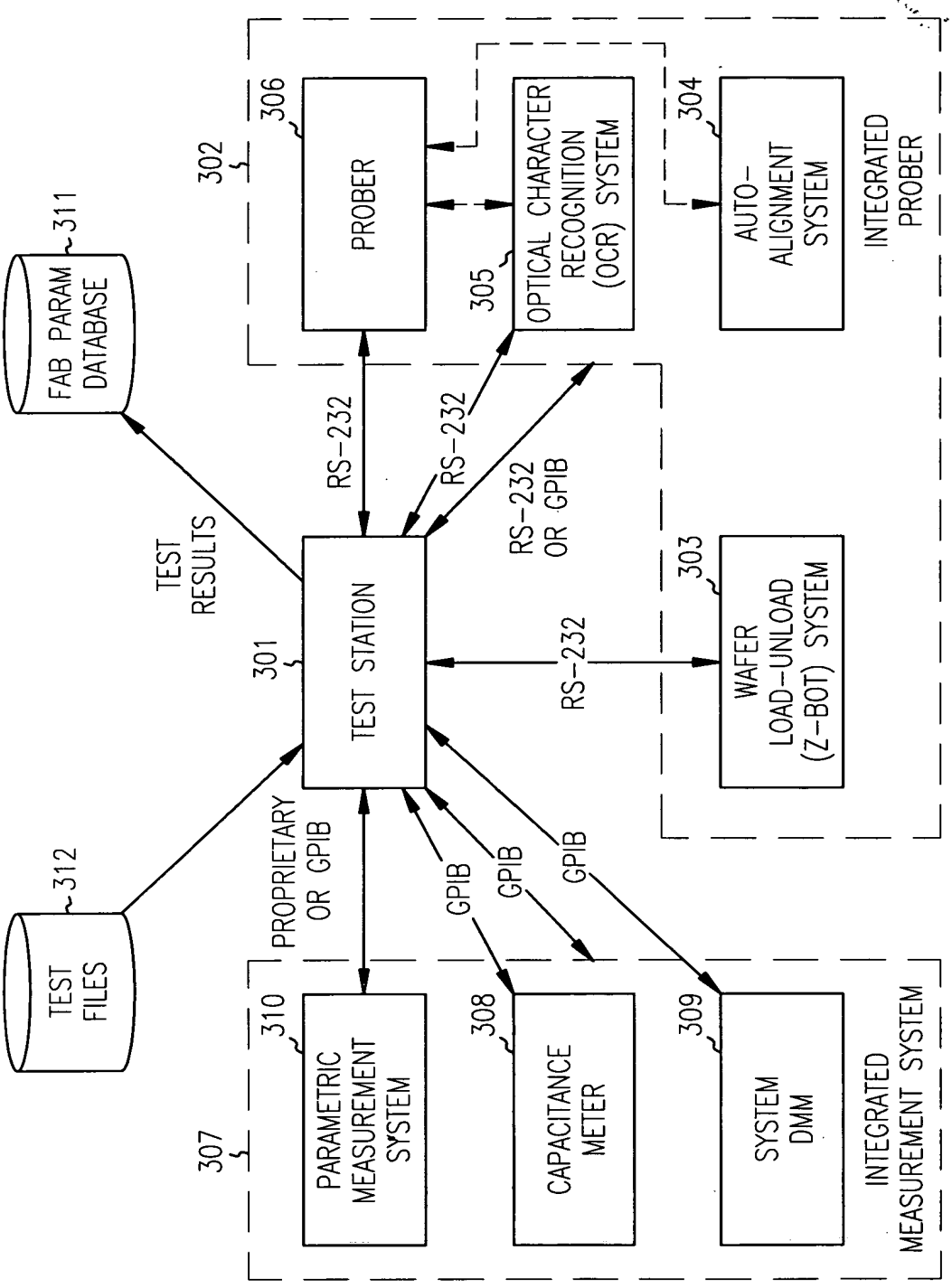

FAB PARAM DATABASE
311
TEST RESULTS
TEST FILES
312
TEST STATION
301
302
PROBER
306
OPTICAL CHARACTER RECOGNITION (OCR) SYSTEM
305
AUTO-ALIGNMENT SYSTEM
304
INTEGRATED PROBER
WAFER LOAD-UNLOAD (Z-BOT) SYSTEM
303
RS-232
RS-232
RS-232 OR GPIB
RS-232
PROPRIETARY OR GPIB
GPIB
GPIB
GPIB
307
PARAMETRIC MEASUREMENT SYSTEM
310
CAPACITANCE METER
308
SYSTEM DMM
309
INTEGRATED MEASUREMENT SYSTEM

FIG. 3

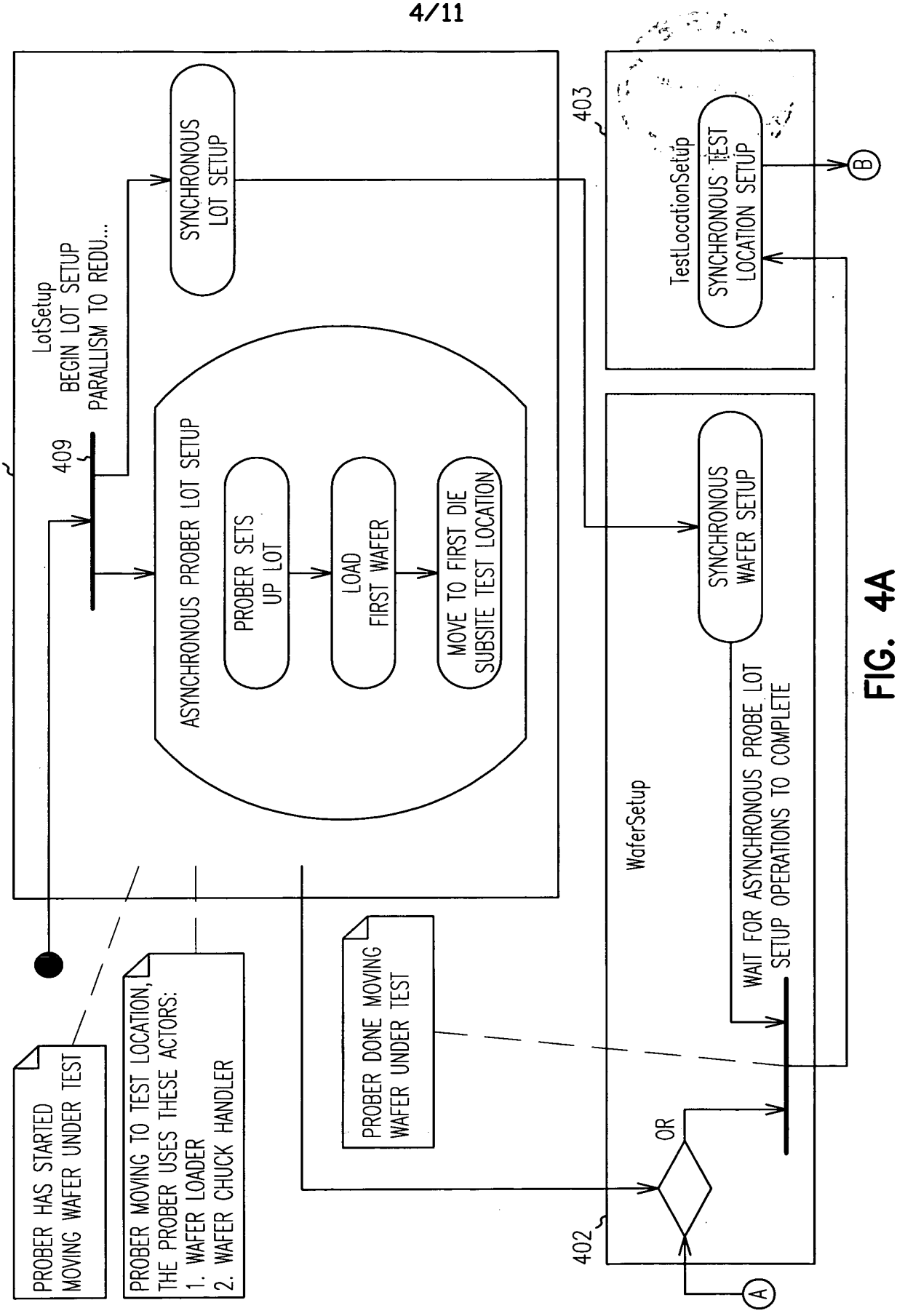

401
LotSetup
BEGIN LOT SETUP
PARALLISM TO REDU...
409
SYNCHRONOUS
LOT SETUP
ASYNCHRONOUS PROBER LOT SETUP
PROBER SETS
UP LOT
LOAD
FIRST WAFER
MOVE TO FIRST DIE
SUBSITE TEST LOCATION
403
TestLocationSetup
SYNCHRONOUS TEST
LOCATION SETUP
B
WaferSetup
SYNCHRONOUS
WAFER SETUP
WAIT FOR ASYNCHRONOUS PROBE LOT
SETUP OPERATIONS TO COMPLETE
OR
402
A
PROBER HAS STARTED
MOVING WAFER UNDER TEST
PROBER MOVING TO TEST LOCATION,
THE PROBER USES THESE ACTORS:
1. WAFER LOADER
2. WAFER CHUCK HANDLER
PROBER DONE MOVING
WAFER UNDER TEST

FIG. 4A

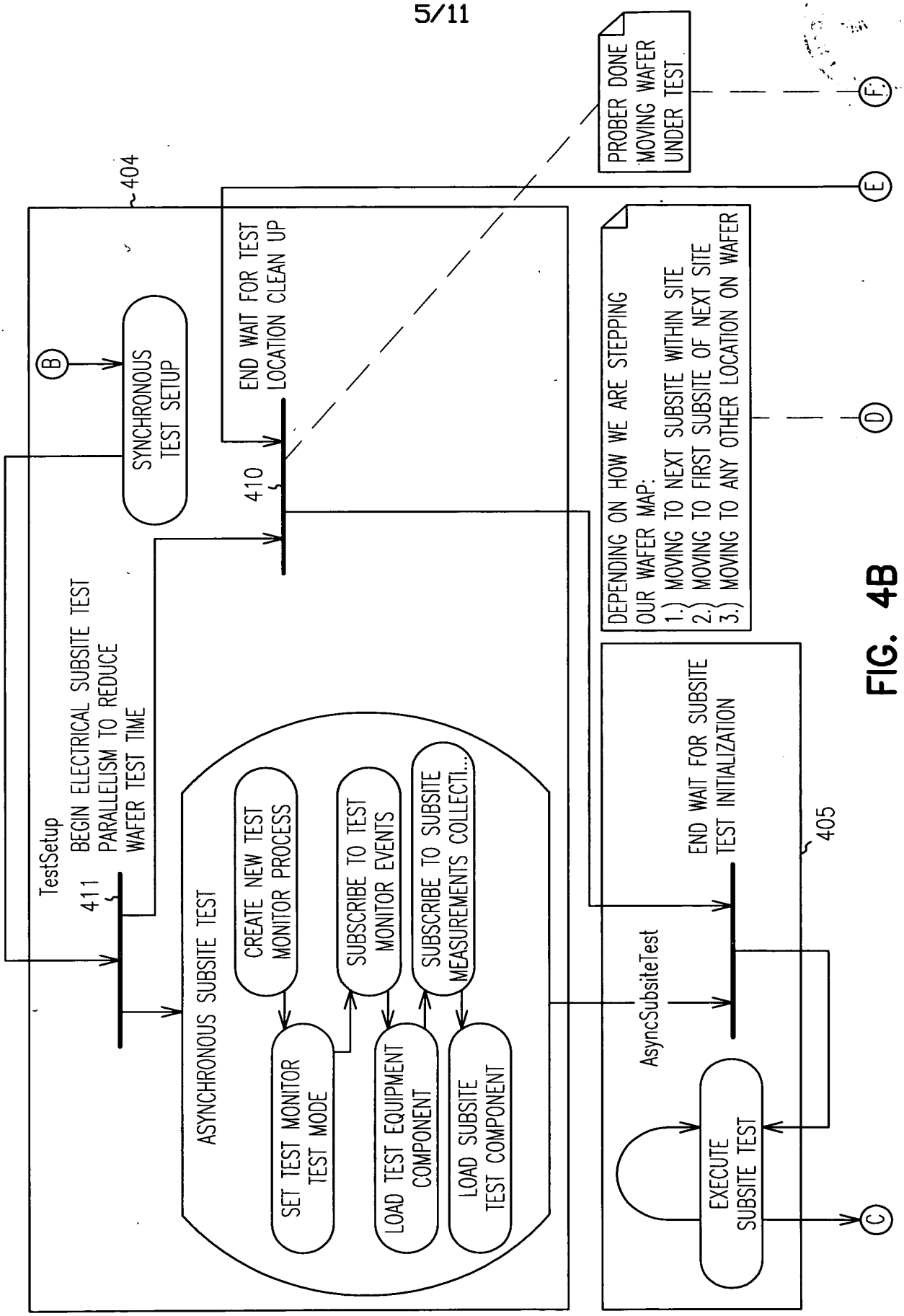

404
B
SYNCHRONOUS TEST SETUP
END WAIT FOR TEST LOCATION CLEAN UP
410
PROBER DONE MOVING WAFER UNDER TEST
E
F
DEPENDING ON HOW WE ARE STEPPING OUR WAFER MAP:
1.) MOVING TO NEXT SUBSITE WITHIN SITE
2.) MOVING TO FIRST SUBSITE OF NEXT SITE
3.) MOVING TO ANY OTHER LOCATION ON WAFER
D
TestSetup
411
BEGIN ELECTRICAL SUBSITE TEST PARALLELISM TO REDUCE WAFER TEST TIME
ASYNCHRONOUS SUBSITE TEST
CREATE NEW TEST MONITOR PROCESS
SUBSCRIBE TO TEST MONITOR EVENTS
SUBSCRIBE TO SUBSITE MEASUREMENTS COLLECTI...
SET TEST MONITOR TEST MODE
LOAD TEST EQUIPMENT COMPONENT
LOAD SUBSITE TEST COMPONENT
END WAIT FOR SUBSITE TEST INITIALIZATION
405
AsyncSubsiteTest
EXECUTE SUBSITE TEST
C

FIG. 4B

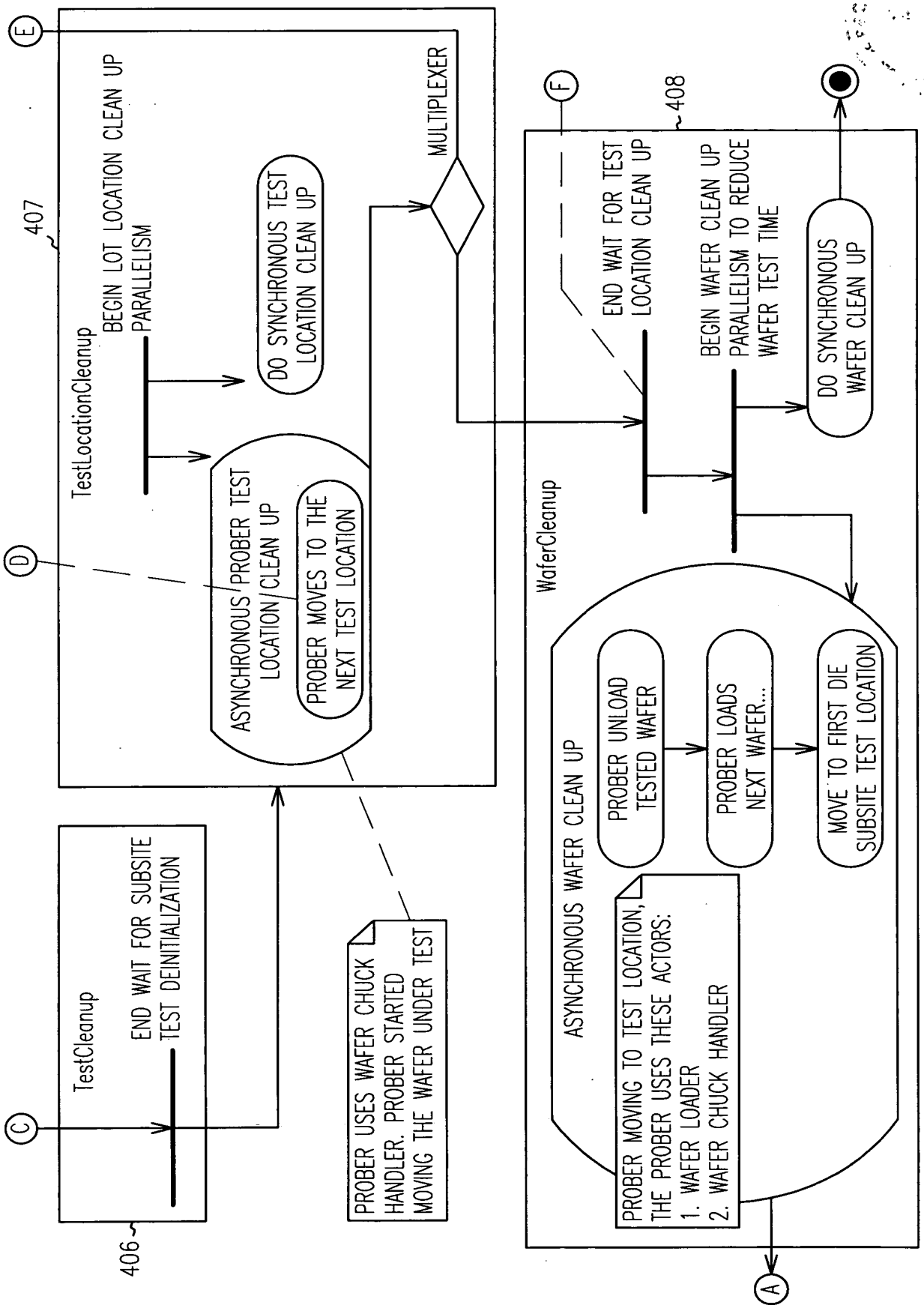

TestCleanup
END WAIT FOR SUBSITE TEST DEINITIALIZATION
406
TestLocationCleanup
BEGIN LOT LOCATION CLEAN UP PARALLELISM
407
DO SYNCHRONOUS TEST LOCATION CLEAN UP
MULTIPLEXER
ASYNCHRONOUS PROBER TEST LOCATION/CLEAN UP
PROBER MOVES TO THE NEXT TEST LOCATION
PROBER USES WAFER CHUCK HANDLER. PROBER STARTED MOVING THE WAFER UNDER TEST
WaferCleanup
END WAIT FOR TEST LOCATION CLEAN UP
BEGIN WAFER CLEAN UP PARALLELISM TO REDUCE WAFER TEST TIME
408
DO SYNCHRONOUS WAFER CLEAN UP
ASYNCHRONOUS WAFER CLEAN UP
PROBER UNLOAD TESTED WAFER
PROBER LOADS NEXT WAFER...
MOVE TO FIRST DIE SUBSITE TEST LOCATION
PROBER MOVING TO TEST LOCATION, THE PROBER USES THESE ACTORS:
1. WAFER LOADER
2. WAFER CHUCK HANDLER
A
C
D
E
F

FIG. 4C

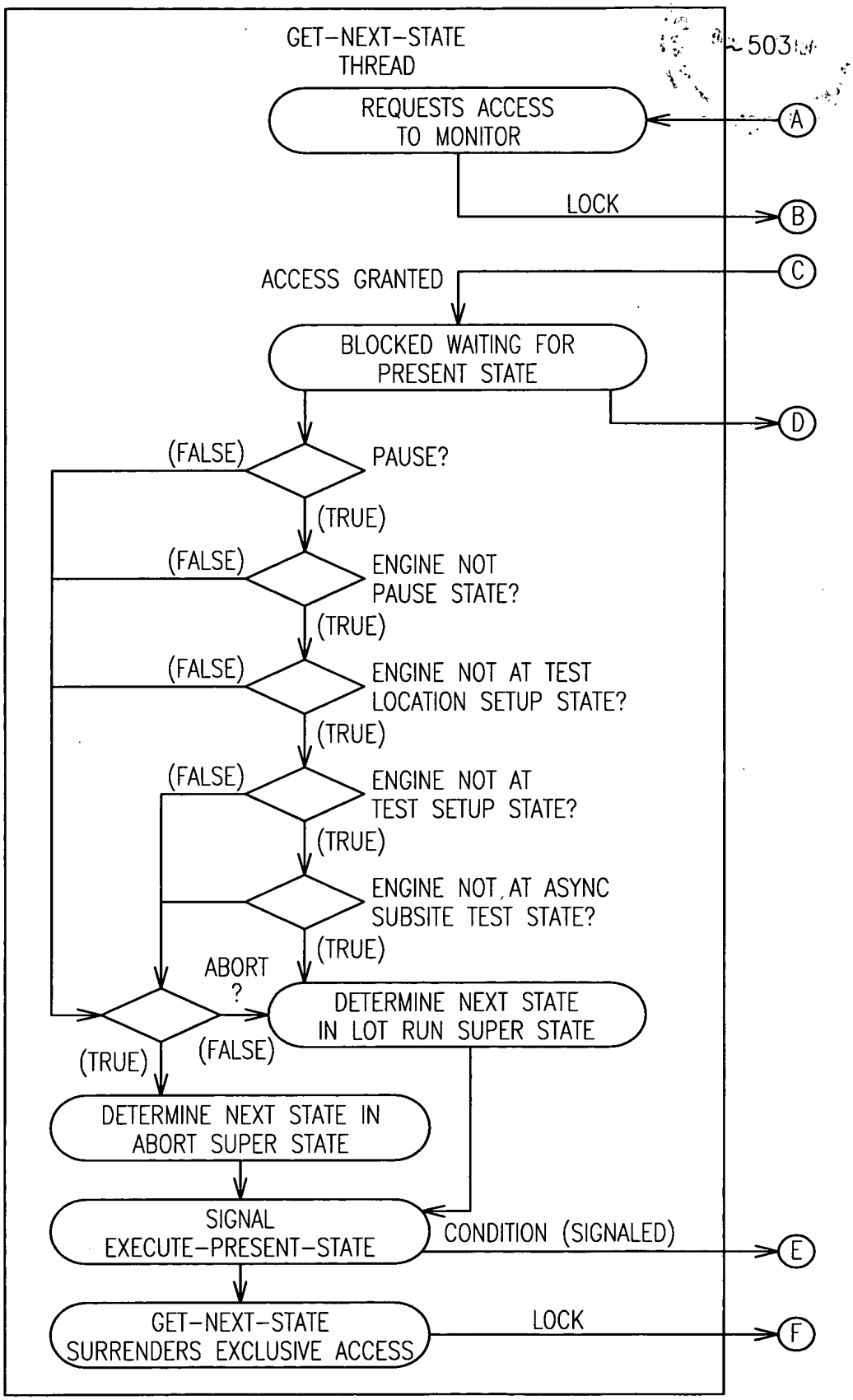

GET-NEXT-STATE THREAD
503
REQUESTS ACCESS TO MONITOR
A
LOCK
B
ACCESS GRANTED
C
BLOCKED WAITING FOR PRESENT STATE
D
(FALSE)
PAUSE?
(TRUE)
(FALSE)
ENGINE NOT PAUSE STATE?
(TRUE)
(FALSE)
ENGINE NOT AT TEST LOCATION SETUP STATE?
(TRUE)
(FALSE)
ENGINE NOT AT TEST SETUP STATE?
(TRUE)
ENGINE NOT AT ASYNC SUBSITE TEST STATE?
(TRUE)
ABORT ?
DETERMINE NEXT STATE IN LOT RUN SUPER STATE
(TRUE)
(FALSE)
DETERMINE NEXT STATE IN ABORT SUPER STATE
SIGNAL EXECUTE-PRESENT-STATE
CONDITION (SIGNALED)
E
GET-NEXT-STATE SURRENDERS EXCLUSIVE ACCESS
LOCK
F

FIG. 5A

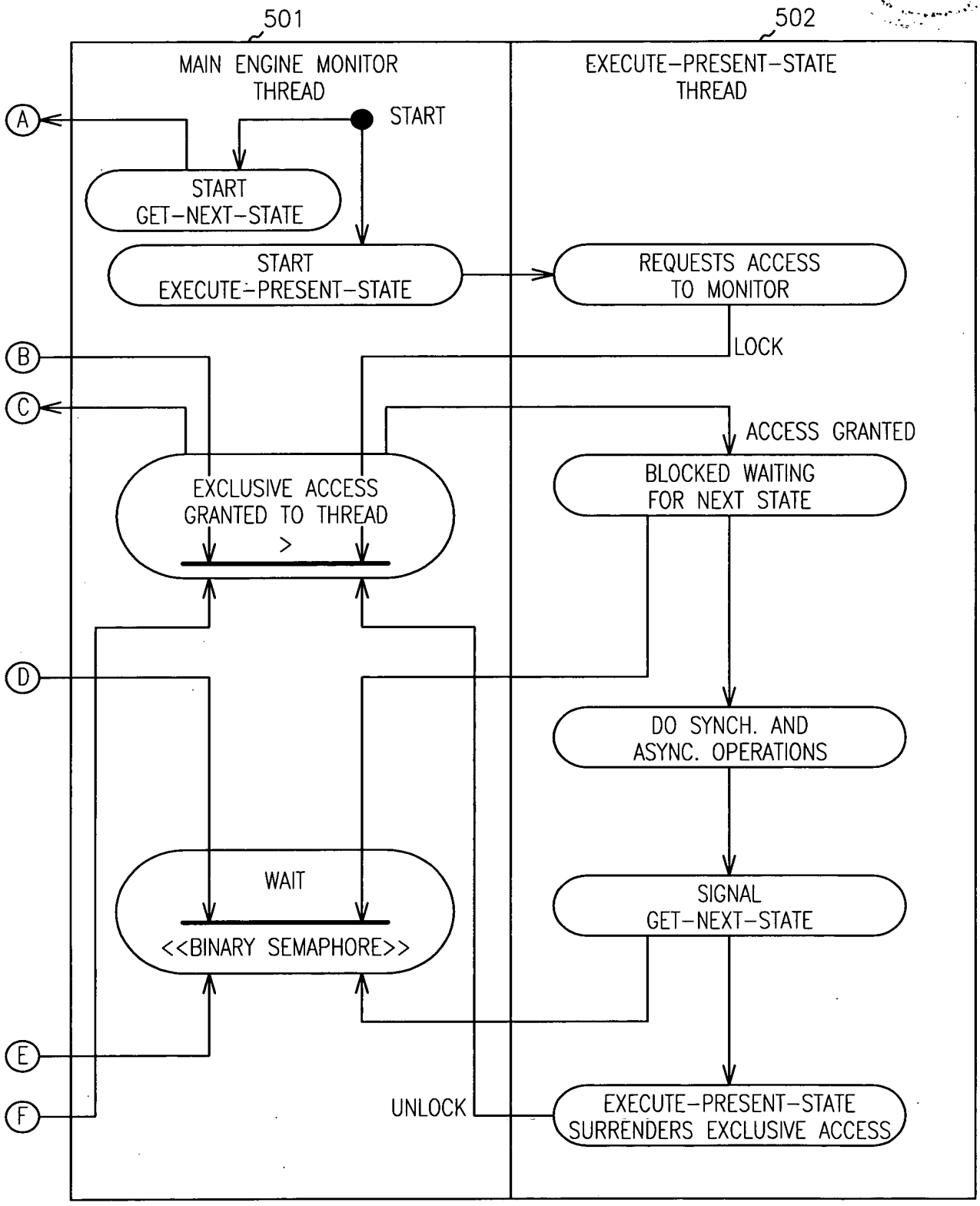
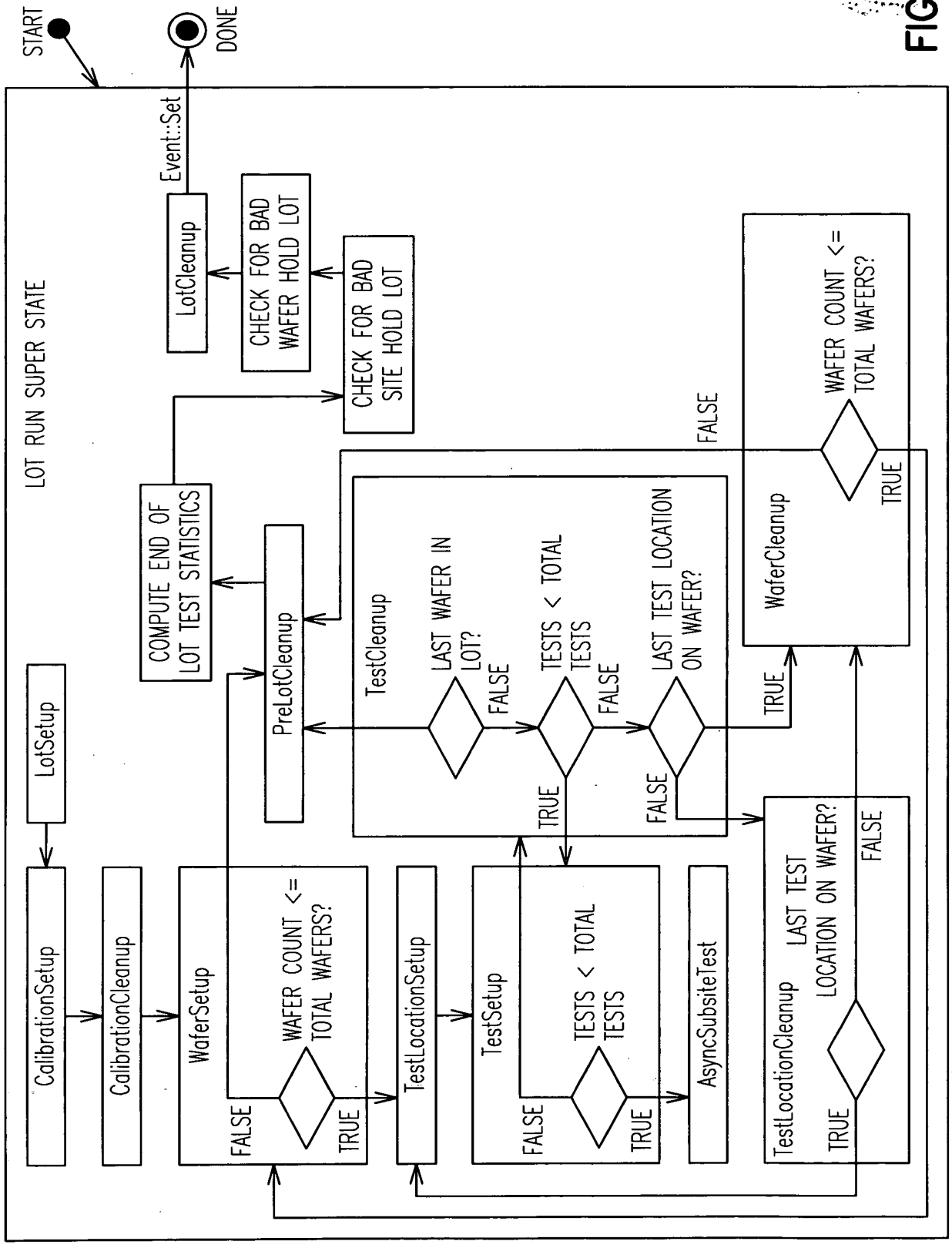

501
502
MAIN ENGINE MONITOR THREAD
EXECUTE-PRESENT-STATE THREAD
A
START
START GET-NEXT-STATE
START EXECUTE-PRESENT-STATE
REQUESTS ACCESS TO MONITOR
LOCK
B
C
ACCESS GRANTED
EXCLUSIVE ACCESS GRANTED TO THREAD
BLOCKED WAITING FOR NEXT STATE
D
DO SYNCH. AND ASYNC. OPERATIONS
WAIT
<<BINARY SEMAPHORE>>
SIGNAL GET-NEXT-STATE
E
F
UNLOCK
EXECUTE-PRESENT-STATE SURRENDERS EXCLUSIVE ACCESS

FIG. 5B

FIG. 6


START
DONE
Event::Set
LOT RUN SUPER STATE
LotCleanup
CHECK FOR BAD WAFER HOLD LOT
CHECK FOR BAD SITE HOLD LOT
COMPUTE END OF LOT TEST STATISTICS
PreLotCleanup
TestCleanup
LAST WAFER IN LOT?
FALSE
TESTS < TOTAL TESTS
FALSE
LAST TEST LOCATION ON WAFER?
TRUE
FALSE
WaferCleanup
WAFER COUNT <= TOTAL WAFERS?
TRUE
FALSE
LotSetup
CalibrationSetup
CalibrationCleanup
WaferSetup
WAFER COUNT <= TOTAL WAFERS?
FALSE
TRUE
TestLocationSetup
TestSetup
TESTS < TOTAL TESTS
FALSE
TRUE
AsyncSubsiteTest
TestLocationCleanup
LAST TEST LOCATION ON WAFER?
TRUE
FALSE

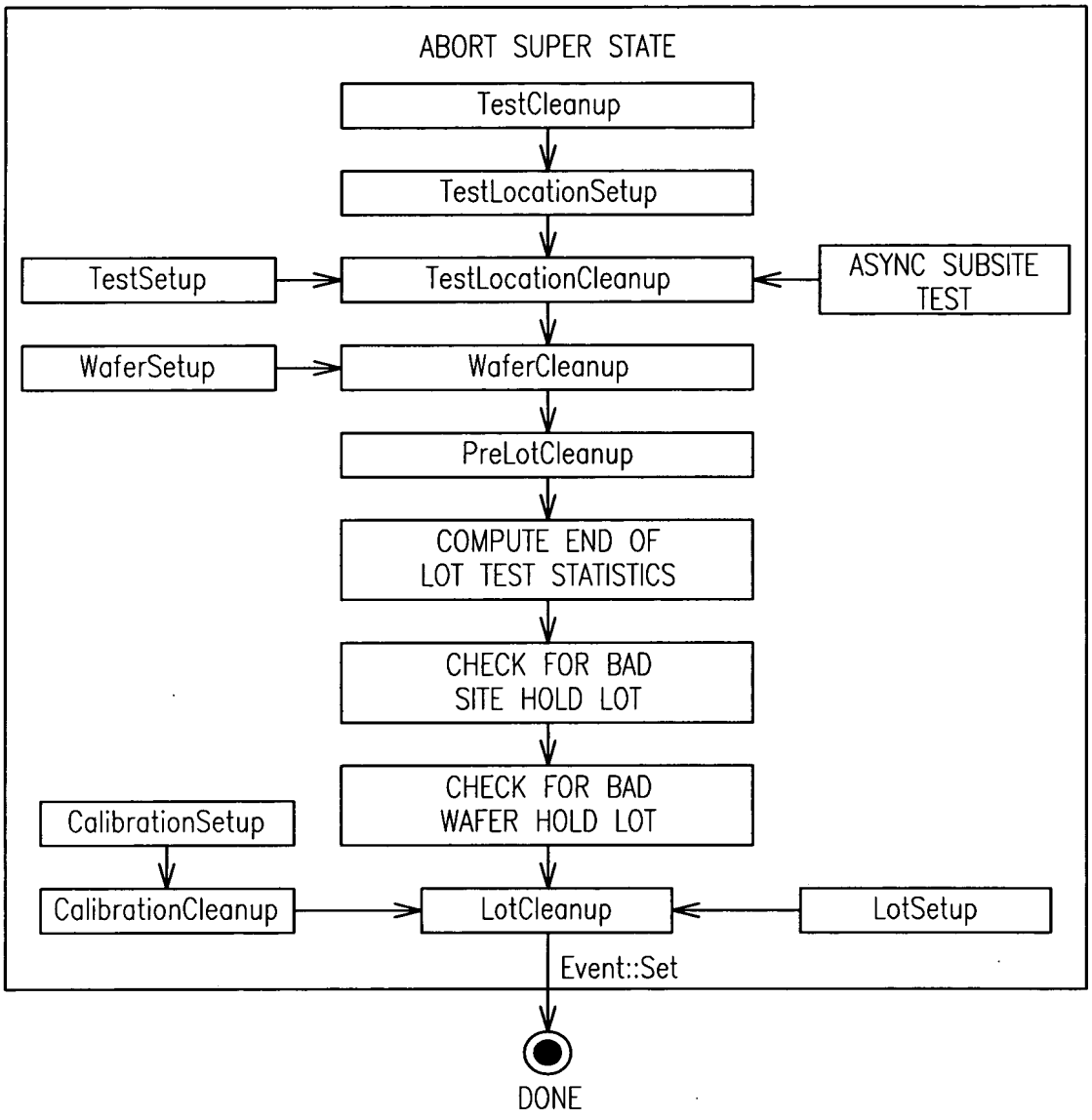

ABORT SUPER STATE
TestCleanup
TestLocationSetup
TestSetup
TestLocationCleanup
ASYNC SUBSITE TEST
WaferSetup
WaferCleanup
PreLotCleanup
COMPUTE END OF LOT TEST STATISTICS
CHECK FOR BAD SITE HOLD LOT
CHECK FOR BAD WAFER HOLD LOT
CalibrationSetup
CalibrationCleanup
LotCleanup
LotSetup
Event::Set
DONE

FIG. 7

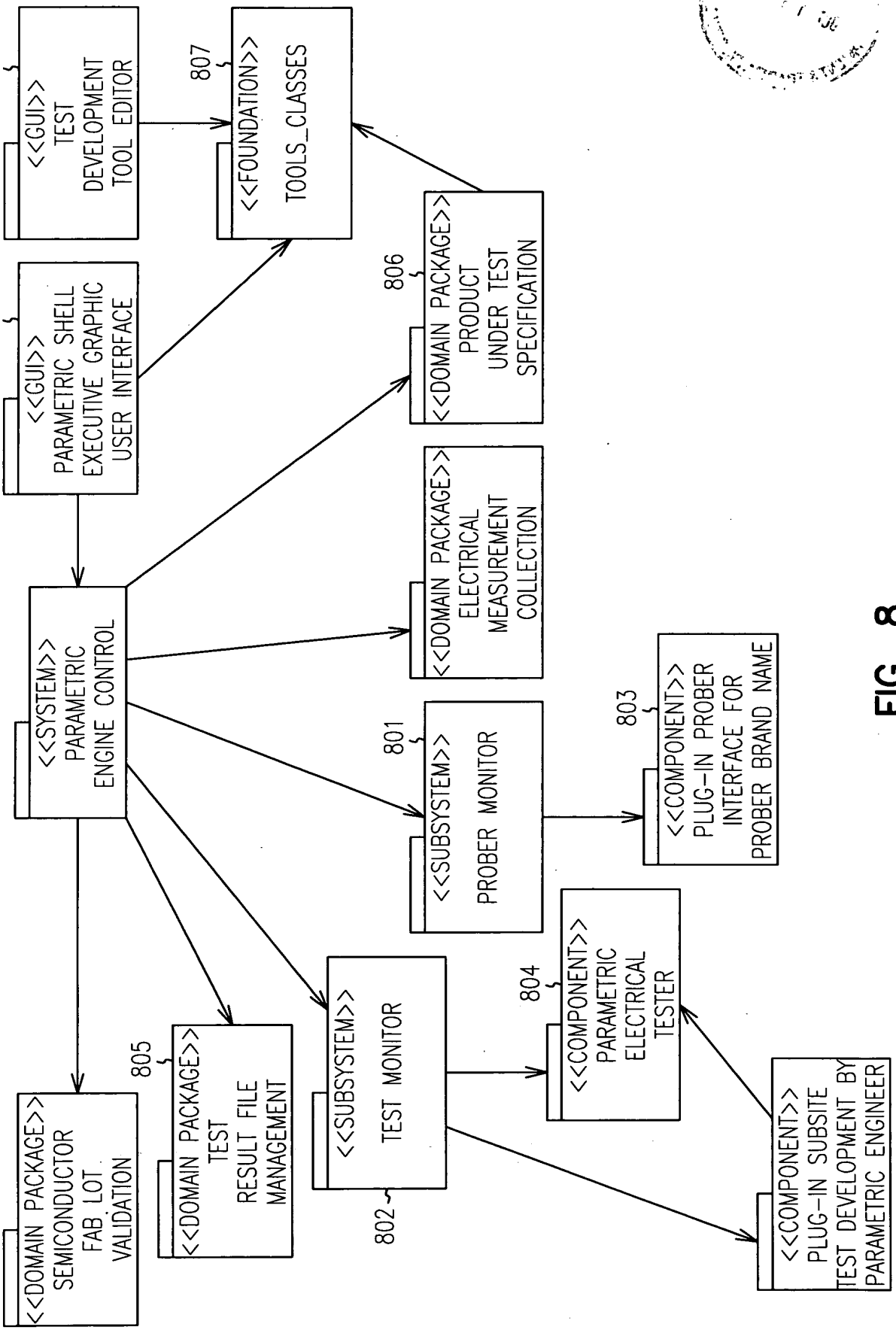

808
<<GUI>>
TEST
DEVELOPMENT
TOOL EDITOR
807
<<FOUNDATION>>
TOOLS_CLASSES
809
<<GUI>>
PARAMETRIC SHELL
EXECUTIVE GRAPHIC
USER INTERFACE
806
<<DOMAIN PACKAGE>>
PRODUCT
UNDER TEST
SPECIFICATION
<<DOMAIN PACKAGE>>
ELECTRICAL
MEASUREMENT
COLLECTION
<<SYSTEM>>
PARAMETRIC
ENGINE CONTROL
801
<<SUBSYSTEM>>
PROBER MONITOR
803
<<COMPONENT>>
PLUG-IN PROBER
INTERFACE FOR
PROBER BRAND NAME
<<DOMAIN PACKAGE>>
SEMICONDUCTOR
FAB LOT
VALIDATION
805
<<DOMAIN PACKAGE>>
TEST
RESULT FILE
MANAGEMENT
<<SUBSYSTEM>>
TEST MONITOR
802
804
<<COMPONENT>>
PARAMETRIC
ELECTRICAL
TESTER
<<COMPONENT>>
PLUG-IN SUBSITE
TEST DEVELOPMENT BY
PARAMETRIC ENGINEER

FIG. 8